ABSTRACT OF THE DISCLOSURE

A signal delay circuit that compensates for other delays introduced within the signal delay circuit itself. A delay-locked loop may produce multiple delayed clock signals, each having a defined phase difference with respect to, and representing a different delay from, a reference clock. A synchronization circuit may determine a first selection value that selects a first delayed clock whose delay compensates for the propagation delays created in a selection circuit. A selection circuit may add a specified offset value to the first selection value to produce a second selection value, and use the second selection value to select a second delayed clock whose delay approximates the sum of the internal delay of the selection circuit and the delay specified by the offset value.